Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845E Chipset Platform for DDR

Design Guide Update

March 2004

Notice: The Intel® 845 chipset family may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the Specification Update.

Document Number: 252737-002

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	September 2003
-002	Add Documentation Change #4. Revise Section 14.1, Schematic Checklist, Host Interface, PWRGOOD	March 2004

Preface

This Design Guide Update document is an update to the specifications and information contained in the *Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845E Chipset Platform for DDR Design Guide*, May 2002, Document Number 298652-001. This Design Guide Update may reference other documents listed in the following Affected Documents/Related Documents table. This document is a compilation of updates to the general design considerations; schematic, layout, and routing updates; and documentation changes. This document is intended for hardware system manufacturers and for software developers of applications, operating systems, and tools. The design guide (and this design guide update) is primarily targeted at the PC market segment and was first published in 2002. Those using this design guide and update should check for device availability before designing in any of the components included in this document.

Information types defined in the Nomenclature section of this document are consolidated into the public design guide update document when the public design guide document is first published. This design guide update document contains a complete list of all known information types.

Affected Documents

Document Title	Document Number
Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845E Chipset Platform for DDR Design Guide, May, 2002	298652-001

Related Documents

Document Title	Document Number
Intel® 845E Chipset Datasheet, Intel® 82845 Memory Controller Hub (MCH), May 2002	290742-001
Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet, May 2002	290744-001

Nomenclature

General Design Considerations include system level considerations that the system designer should account for when developing hardware or software products using the Intel® 845E Chipset: 82845 Memory Controller Hub (MCH).

Schematic, Layout, and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Codes Used in Summary Table

Doc:	Document change or update that will be implemented.
Shaded:	This item is either new or modified from the previous version of the document.

NO.	Plans	GENERAL DESIGN CONSIDERATIONS
		There are no General Design Consideration changes in this Design Guide Update revision.

NO.	Plans	SCHEMATIC, LAYOUT, AND ROUTING UPDATES
		There are no Schematic, Layout, and Routing Update changes in this Design Guide Update revision.

NO.	Plans	DOCUMENTATION CHANGES
1	Doc	Corrected CLK 408 Pin Names
2	Doc	Modified Section 14.8, Power and Ground Checklist
3	Doc	Changed Section 14.5, Intel® ICH4 Interface Checklist
4	Doc	Revise Section 14.1, Schematic Checklist, Host Interface, PWRGOOD

General Design Considerations

There are no General Design Considerations in this Design Guide Update revision.

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Schematic, Layout, and Routing Updates

There are no Schematic, Layout, and Routing Update changes in this Design Guide Update revision.

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Documentation Changes

1. CLK408 Pin Names

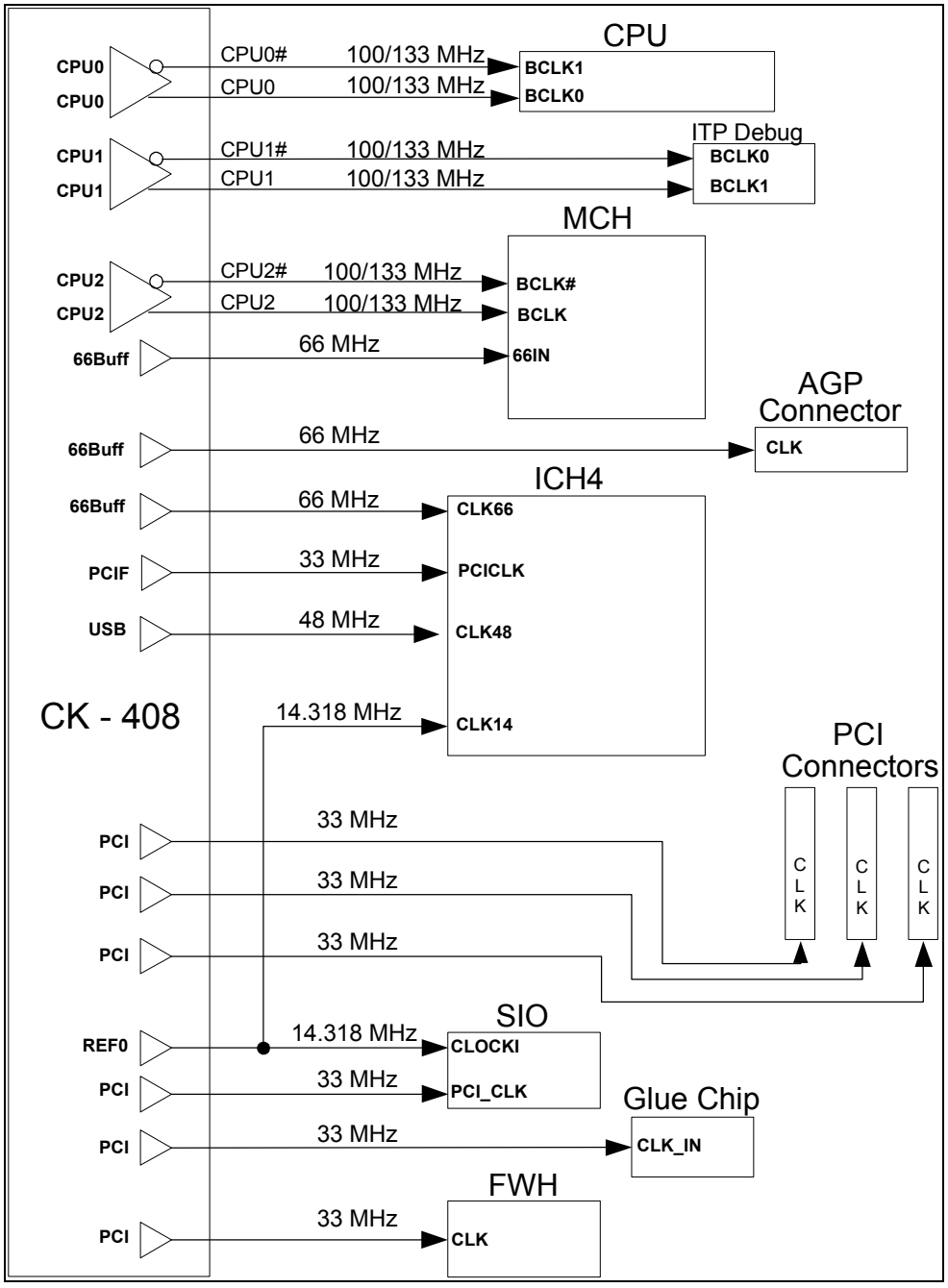
(1) Reference Section 11.1, Clock Generation. Replace Table 11.2, Platform System Clock Cross-Reference, with the following new table:

Table 11.2. Platform System Clock Cross-Reference

Clock Group	CK-408 Pin	Component	Component Pin Name
HOST_CLK	CPU0	CPU	BCLK0
	CPU0#	CPU	BCLK1
	CPU1	ITP Debug Port	BCK
	CPU1#	ITP Debug Port	BCK#
	CPU2	MCH	BCLK
	CPU2#	MCH	BCLK#
CLK66	66BUFF	MCH	66IN
		ICH4	CLK66
AGPCLK	66BUFF	AGP Connector or AGP Device	CLK
CLK33	PCIF	ICH4	PCICLK
	PCI	SIO	PCI_CLK
	PCI	Glue Chip	CLK_IN
	PCI	FWH	CLK
CLK14	REF0	ICH4	CLK14
		SIO	CLOCKI
PCICLK	PCI	PCI Connector #1	CLK
		PCI Connector #2	CLK
		PCI Connector #3	CLK
USBCLK	USB	ICH4	CLK48

(2) Replace Figure 11-1, Clock Topology, with the following new figure:

Figure 11-1. Clock Topology



(3) Reference Section 14.7, Clock Interface CK_408. Replace the CPU2 and CPU2# Checklist Items with the following:

CPU2	• Connect to **BCLK** in MCH • Connect to a series 27.4 Ω ± 1% resistor and terminate to GND through a 49.9 Ω ±1% resistor	
CPU2#	• Connect to **BCLK#** in MCH • Connect to a series 27.4 Ω ± 1% resistor and terminate to GND through a 49.9 Ω ±1% resistor	

2. Section 14.8, Power and Ground Checklist

Reference Section 14.8, Power and Ground IChecklist.

(1) In the "Description" section of the V5_REF Checklist Item, add the following: "V5_REF must be connected properly for USB2 to work."

(2) In the "Description" section of the V5_REF_Sus Checklist Item, add the following: "V5_REF_Sus must be connected properly for USB2 to work."

3. Section 14.5, Intel® ICH4 Interface Checklist

Change the first bullet in the "Description" of the ICH4 Interrupt Interface Items of the INTRUDER# Checklist Item to: "This signal requires a very weak pull-up to the RTC power well. Pull signal to VCCRTC (VBAT) through a 330K Ohm resistor."

4. Revise Section 14.1, Schematic Checklist, Host Interface, PWRGOOD

Revise Section 14.1, Schematic Checklist, Host Interface, PWRGOOD, with the following:

Signal	Description
PWRGOOD	Connects to ICH4 CPUPWRGD pin. Note that a weak pullup to VCCP (V_CPU_IO) is required and that such value should not exceed ICH4s Ioh2/Iol2 specs.